POWER EFFICIENT TRUNCATION AND ROUNDING-BASED SCALABLE APPROXIMATE MULTIPLIER USING CLA

A Project report submitted to Jawaharlal Nehru Technological University, GV in the partial fulfillment of the requirements for the award of degree of

BACHELOR OF TECHNOLOGY

In

ELECTRONICS AND COMMUNICATION ENGINEERING

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DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

iis is to certify that the project entitled "**POWER EFFICIENT TRUNCATION AND OUNDING-BASED SCALABLE APPROXIMATE MULTIPLIER USING CLA**" is being submitted : the partial fulfillment of requirements for the award **Bachelor of Technology** in **Electronics & ommunication Engineering** is a bonafide work done by **G.LAHARI(20811A0420), B.MAHESH BABU 0811A0411), B.NIKHIL TEJA(20811A0414), K.PRASANNA(20811A0429), K.TEJA(20811A0431)** under my guidance during 2023-2024 and it has been found suitable for acceptance according to the quirements of the University.

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INTERNAL GUIDE

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ABSTRACT

The modern world is running forward in achieving the challenge of minimum area. So many efficient structures are employed in the traditional designs so that the max speed can be included. Most of the structures will have multiplier as the basic blocks, which will run with less speed because of its huge structure. In practical, not all applications need accurate results such as in image processing and digital signal processing etc. So approximate multipliers are employed. By considering these two points a scalable approximate multiplier, called truncation- and rounding-based scalable approximate multiplier (tosam) is presented, which reduces the number of partial products by truncating each of the input operands based on their leading one-bit position. In the proposed design, multiplication is performed by shift, add, and small fixed-width multiplication operations resulting in large improvements in the speed compared to those of the conventional multiplier. To improve the total accuracy, input operands of the multiplication part are rounded to the nearest odd number. Because input operands are truncated based on their leading one-bit positions, the accuracy becomes weakly dependent on the width of the input operands and the multiplier becomes scalable. Higher improvements in design parameter (less area and power) are observed.